Docket No.: W&B-INF-952

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant

ROBERT KAISER ET AL.

Filed

CONCURRENTLY HEREWITH

Title

INTEGRATED CIRCUIT HAVING A DATA PROCESSING UNIT

AND A BUFFER MEMORY

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks, Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent 5,313,424 (Adams et al.), dated May 17, 1994;

German published Non-Prosecuted Patent Application DE 197 08 965 A1 (Zettler), dated September 24, 1998, data storage;

Tarr M. et al.: "Defect Analysis System Speeds Test and Repair of Redundant Memories", Electronics, January 12, 1984, pp. 175, 177, 179;

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications. patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

For Applicants

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Date: December 20, 2001

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SHEET 1 OF 1

FORM PTO-1449 (SUBSTITUTE)				Attorney Docket No.: W&B-INF-952 Appl. No.				
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE								
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant ROBERT KAISER ET AL.				
(37 CFR 1.98(b))				Filing Date December 20, 2001 Group Art Unit				
EXAMINER INITIALS	ĺ	PATENT NO.	DATE	PATENTEE	CLASS	SUB		ING TE
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	Tarr M. et al.: "Defect Analysis System Speeds Test and Repair of Redundant Memories", Electronics, January 12, 1984, pp. 175, 177, 179;							
EXAMINER			DATE CONSIDERED					
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.								